

FS2 CLAM[®]

FAQ

For Actel ProASIC^{PLUS} Devices

September 29, 2003



First Silicon Solutions, Inc.
4000 SW Kruse Way Place, Bldg. 3, Suite 210
Lake Oswego, OR 97035
Voice: +1-503-489-0311
Fax: +1-503-489-0315
<http://www.fs2.com>
info@fs2.com
support@fs2.com

Table of Contents

- 1. WHAT IS THE CLAM? 3
- 2. IS THERE MORE THAN ONE VERSION OF THE FS2 CLAM PROBE? 3
- 3. WHAT IS THE DIFFERENCE BETWEEN THE EXTERNAL AND INTERNAL VERSIONS OF THE CLAM IP? 3
- 4. WHAT IS THE DIFFERENCE BETWEEN THE 1X, 2X AND 4X CONFIGURATIONS OF THE EXTERNAL CLAM IP? 3
- 5. IS THE CLAM IP AVAILABLE IN BOTH VERILOG AND VHDL? 4
- 6. HOW DO I SET UP MY DESIGN TO USE EITHER EXTERNAL OR INTERNAL CLAM IP? 4
- 7. HOW DO I USE THE 1X, 2X OR 4X CONFIGURATION OF THE EXTERNAL CLAM IP IN MY DESIGN? 4
- 8. HOW MANY SIGNALS CAN THE FS2 CLAM SIMULTANEOUSLY MONITOR? 4
- 9. WHAT SIZE TRACE MEMORY DOES THE CLAM IP SUPPORT? 4
- 10. HOW MANY TRIGGER EVENTS ARE SUPPORTED? 4
- 11. WHICH ACTEL DEVICES ARE SUPPORTED? 4
- 12. WHICH EDA TOOLS ARE SUPPORTED? 5
- 13. WHAT ARE THE MINIMUM AND MAXIMUM CLOCK FREQUENCIES THAT THE CLAM SUPPORTS? 5
- 14. HOW MANY LOGIC TILES DOES THE CLAM IP USE? 5
- 15. IS IT NECESSARY TO ADD SYNTHESIS CONSTRAINTS FOR THE CLAM IP TO MEET TIMING? 6
- 16. IS THERE A DEMO DESIGN AVAILABLE? 6
- 17. HOW DO I CUSTOMIZE THE CLAM IP? 6
- 18. WHERE CAN I GET MORE DETAILED INFORMATION ON HOW TO USE THE CLAM IP IN MY DESIGN? 6

FS2, OCI, and CLAM are registered trademarks of First Silicon Solutions. All other trademarks are the properties of their respective owners.

1. What is the CLAM?

The FS2 CLAM[®] (Configurable Logic Analyzer Module) System consists of IP logic and external hardware and software. It is designed to work as a logic analyzer for Actel ProASIC and ProASIC^{PLUS} FPGAs. It routes internal signals in the designer's HDL code to a trace memory where the signals can be examined. Trigger events and other configuration parameters can be set up by the designer to control which signals are recorded in memory and the conditions for capture.

2. Is there more than one version of the FS2 CLAM Probe?

Yes, there are two versions, one for use with the Internal configurations of the CLAM IP and one for use with both the Internal and External versions of the CLAM IP. The Internal version of the CLAM Probe is not compatible with the External version of the CLAM IP.

3. What is the difference between the External and Internal versions of the CLAM IP?

The External Clam IP contains no event recognition logic and uses no on-chip memory to trace data, which makes for an extremely low impact to the area requirements on the user's design. Instead, all data is routed off-chip to an FS2 CLAM Probe. The CLAM Probe has complex event recognition logic enabling the designer to create complex trigger events. The Probe also has an extensive trace memory allowing the designer to store large amounts of data without using any additional on-chip resources.

The Internal Clam IP uses event recognition logic and trace memory in the designer's chip to hold trace data and control logic to start, stop and read the trace memory. The benefit of using the Internal version of the CLAM IP is that it only requires 2 external device pins on the chip, independent of how many signals are being traced. The External CLAM IP requires from 2 to 35 external device pins, depending on the configuration and the number of signals being traced. When used with the internal CLAM, the FS2 Probe is used to configure the CLAM control logic on the chip and to route data from the on-chip trace to a Windows PC.

4. What is the difference between the 1x, 2x and 4x configurations of the External CLAM IP?

The External CLAM comes in 3 different configurations: 1x, 2x and 4x. The 2x and 4x configurations of the CLAM can be used to reduce the number of package I/O pins required by the CLAM but still allows for trace memory and event control to be located in the FS2 CLAM Probe.

In the 1x configuration, a single, system wide clock is used for all data and control registers as well as the data I/O registers, which drive the external device pins used by the CLAM. The number of device I/O pins required on the package by the 1x configuration of the Clam IP will be equal to the number of data signals being traced plus control signals.

In the 2x configuration, the CLAM IP uses two clocks. One is used to clock the control and data registers within the CLAM. This is the system clock, just like in the 1x configuration. The second clock is used to clock the data I/O registers and operates at twice the frequency of the system clock. In order to reduce the number of I/O pins required by the CLAM IP, the CLAM multiplexes the trace data to the I/O pins such that data is being clocked at twice the frequency of the system clock, but at half the width. The number of data I/O pins required by the 2x configuration is half that of the 1x configuration.

In the 4x configuration, the CLAM IP again uses two clocks. The first is used to clock the control and data registers within the CLAM. This is the system clock, just like in the 1x configuration. The second clock is used to clock the data I/O registers and operates at 4 times the frequency of the system clock. In order to reduce the number of I/O pins required by the CLAM IP, the CLAM multiplexes the trace data to the I/O pins such that data is being clocked at 4 times the frequency of the system clock, but at 1/4 the width. The number of data I/O pins required by the 4x configuration is 1/4 that of the 1x configuration.

5. Is the CLAM IP available in both Verilog and VHDL?

Yes. Both Verilog and VHDL design flows are fully supported. Verilog and VHDL source file sets are available for both the Internal and External CLAM IP.

6. How do I set up my design to use either External or Internal CLAM IP?

The CLAM probe hardware and cable connectors are different between the internal trace and external trace systems. A designer needs to first determine which system is appropriate for the design. The designer then instantiates the internal or external module in the design as required. If there is some doubt about which design to use, then the External CLAM probe should be chosen since it can be connected to the External or Internal CLAM IP. The External CLAM uses a 38 pin Mictor connector but it can be routed to pins on the FPGA for either on-chip or off-chip use. The Mictor cable on the External probe can also be used with a 10 pin adapter to connect to standard on-chip 10 pin target connectors.

7. How do I use the 1x, 2x or 4x configuration of the External CLAM IP in my design?

A designer can select which configuration of the CLAM IP his or her design will use simply by instantiating the desired module in his or her code. All three configurations are provided and supported with the External CLAM IP.

8. How many signals can the FS2 CLAM simultaneously monitor?

The CLAM can simultaneously monitor one input set consisting of up to 32 signals. However, up to 4 input sets can be routed into the clam. The user can configure the CLAM via the FS2 software at run time to select which of the 4 input sets is to be monitored. This gives a total of up to 128 signals, which can be selectively monitored.

9. What size trace memory does the CLAM IP support?

The External CLAM supports memory depth of 128K words.

The Internal CLAM supports trace memory depth from 2 words to 4K words.

10. How many trigger events are supported?

The External CLAM IP supports 4 trigger events.

The Internal CLAM IP is configurable for 0, 1 or 2 trigger events determined when the designer instantiates the Verilog or VHDL code into the design.

11. Which Actel devices are supported?

The FS2 CLAM IP has been verified in simulation and in hardware on the Actel ProASIC^{PLUS} family of devices. However, the CLAM IP contains no code that is specific to the ProASIC^{PLUS} device line. It is entirely possible that the CLAM IP will function well in other Actel technologies, but this has not been verified by FS2.

12. Which EDA tools are supported?

The FS2 CLAM IP has been verified by FS2 to flow without error through the Actel Libero software. This includes Modeltech ModelSim for simulation and Synplicity Synplify Light for synthesis.

13. What are the minimum and maximum clock frequencies that the CLAM supports?

Below is a table showing the minimum and maximum frequencies for different versions of the CLAM IP.

Table 3. CLAM IP Timing Specifications

CLAM Version	Max Trace Width	Min System Frequency	Max System Frequency	Max Output Width	Max Output Frequency
1X	32	50 MHz	100 MHz	32	100 MHz
1X-slow	32	0.0 MHz	50 MHz	32	25 MHz
2X	32	25 MHz	100 MHz	16	200 MHz
2X-slow	32	0.0 MHz	25 MHz	16	25 MHz
4X	32	12.5 MHz	33 MHz	8	132 MHz
4X-slow	32	0.0 MHz	12.5 MHz	8	25 MHz
Internal	32	560 KHz	Depends on technology	NA	NA

14. How many logic tiles does the CLAM IP use?

Below is a table showing the approximate area requirements for different configurations of the External CLAM.

Table 1. Area Requirement for the External CLAM IP vs. Different Configurations

Version	TRACE_WIDTH	Logic Tiles Used
1x	32	132
1x	16	72
1x	8	36
2x/4x	32	167
2x/4x	16	91
2x/4x	8	47

Below is a table showing the approximate area requirements for different configurations of the Internal CLAM.

Table 2. Area Requirement for the Internal CLAM IP vs. Different Configurations

TRACE_WIDTH	Number of Events	Logic Tiles Used
32	2	1627
16	2	1020
8	2	708
32	1	1202
16	1	797
8	1	585
32	0	690
16	0	536
8	0	449

15. Is it necessary to add synthesis constraints for the CLAM IP to meet timing?

In order for the FS2 CLAM IP to meet the timing specifications listed in table 1, it will be necessary to add timing constraints to the design. The FS2 Simulation and Synthesis Guide for Actel ProASICPlus Devices contains a detailed explanation and examples of the constraints that should be included.

16. Is there a demo design available?

Yes. The code for a fully operational top-level design is included in the file sets for both Verilog and VHDL. A designer is free to use this design as a starting point or a reference if desired.

17. How do I customize the CLAM IP?

The CLAM code is parameterized such that the designer can fully customize the CLAM IP by driving the desired parameter values from his or her code, without the need to alter a single line of code within the FS2 CLAM. FS2 does not recommend that a designer make changes to the CLAM IP.

18. Where can I get more detailed information on how to use the CLAM IP in my design?

The FS2 CLAM Instantiation, Simulation and Synthesis Guide is included in the IP file set from FS2. It contains a detailed description, along with examples, of how to use the CLAM IP in your design.