



First Silicon Solutions

## Technical Data for **SNAV-186**

### System Navigator for ARC International (formerly VAutomation) V186 and Turbo186 Synthesizable Cores

The System Navigator supports the family of Turbo 186 cores used in processors from suppliers including Lantronix. VAutomation was acquired by ARC International in 2000. Processors based on the design are available from Lantronix and Grid Connect.

The System Navigator for Turbo 186 cores is designed to support the special features and integrated peripherals of the synthesizable core. Special "silicon hooks" for System-on-Chip development are integrated into the synthesizable IP model for the core. These On-Chip Instrumentation (OCI™) extensions allow FS2 to provide a powerful debug tool with advanced features at a competitive price.

The System Navigator is contained in a compact chassis that connects to the target system using a standard 10 pin connector. It requires access to only 4 pins in the core processor. The system runs on a Windows® 2000/XP PC over a USB 2.0 port (10/100 Ethernet optional). An optional graphical, source level debugger program, from Paradigm Systems provides an intuitive, easy to use interface.

#### **Software Breakpoints**

An unlimited number of software breakpoints can be set anywhere in the physical address space of the processor. The software breakpoints use a unique opcode, which leaves the INT3 vector available to the user or another debugger on the target system.

#### **Hardware Event Recognizers**

The OCI debug block in the CPU core provides 4 event recognizers that can generate triggers to control breakpoints and trace collection. The most basic use of recognizers is for hardware execution breakpoints. Unlike software breakpoints, hardware execution breakpoints can be set in ROM or FLASH memory. Like their software counterparts,

they stop program execution just prior to an instruction being executed.

#### **Features Overview**

- Utilizes On-Chip Instrumentation (OCI™) debug extensions in the synthesizable core
- Read-write all CPU registers, memory, and I/O
- Go, halt processor run control
- Single step by assembly or C source instruction
- Unlimited software breakpoints (not Interrupt 3)
- Load binary, Intel Hex or OMF86 file formats
- Debug register breakpoints for code and data
- Low-level access to JTAG functions for silicon verification
- Flash programming support
- Easily program and modify integrated peripherals
- Single line assembler and disassembler
- Trace window with full trace decode into instruction mnemonics
- Symbolic debug
- Load symbols, including code, variables, and variable types
- Support C and assembly source code
- Source window can display C source or mixed mode
- Source window provides execution control: go; halt; goto cursor; step over/into call
- Source window can set or clear software or hardware breakpoints
- Source window allows selecting global or local variable and adding to variable window
- Trigger window for setting complex triggers
- Macros supporting C expressions and operators



## Complex Trigger Features

For more sophisticated debugging, the event recognizers can monitor bus activity to program memory, data memory and cycle types. They can control breakpoints and trace collection “event actions”. Event recognizers can be combined to provide two “super events”. Super events can be configured in “arm”, “range”, or “mask” modes. In arm mode, the first event of the event pair must be satisfied before the second event is activated. In range mode, the super event looks for an address range instead of a single address. In mask mode, the super event looks for specific address and data values, both of which can include masking bits.

## Real Time Trace

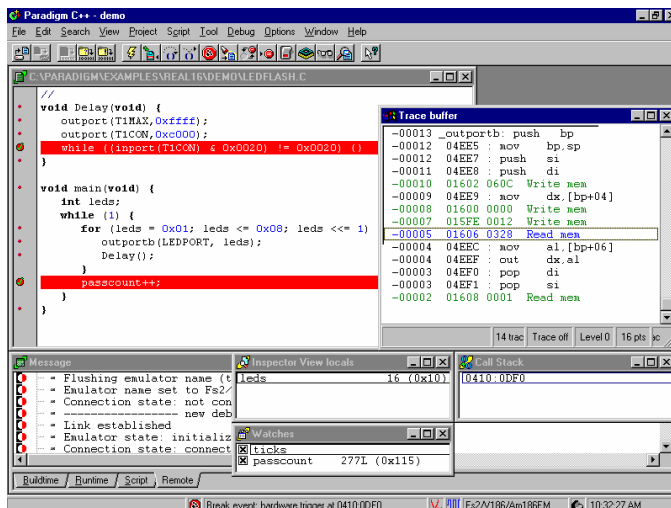
Trace is collected in one of three modes: Cycle, Branch or Timer. Cycle mode collects bus cycles generated by the core or DMA unit. Branch mode collects execution path changes. The Branch trace display contains disassembled executed instructions. The traced instructions are related back to the C code in the source window. Trace depth can be scaled by powers of 2 from 0 to 256 frames. The effective trace depth can be larger depending on the number of branches taken or not taken in the program. Timer mode records a frame with a timestamp each time a trigger is satisfied.

## Scaled Solutions

Because many SoC designs have both power and gate limitations, FS2 has provided a scaled solution. Debug extensions in the processor core are initially in the “power-off” state. Connecting the debugger causes the extensions to power-on. Debug extensions can be scaled to control gate count. The benefit is fewer gates for lower power and core size while trading off debug capability. Either 1,2, or 4 event recognizers can be used. With one event recognizer, trigger definitions are limited to a single address and cycle type.

## Source Level Debug

An available option with the VSA-8X/18X is the Paradigm Systems C/C++ compiler and debugger tool suite. The Windows interface is tightly integrated to the VSA trigger and trace facilities. It includes a C-like macro language supporting automation of routine tasks or regression tests. It



allows the user to test CPU parameters, initiate actions, and supports passing of parameters. The Paradigm package includes the Borland C/C++ compiler, assembler and utilities. The package supports 24-bit addressing for programs up to 16 MB.

## FS2 Command line interface

The System Navigator includes a command line interface (CLI). The CLI can be used as both a user interface and also for writing sophisticated automated sequences of tasks for items like regression tests. The CLI is based on the widely used Tcl/tk command language.

## Testing

A comprehensive self-test capability is included with the system. For system verification, a loop-back board is provided which is plugged onto the target interface cable. A self-test exercises internal nodes and tests to insure the cable signal integrity.

## Host Requirements

PC with USB 2.0 or 10/100 Ethernet connection. Windows® 2000 or XP operating system are required.

**Order Code:** SNAV-186- USB (ETH)



First Silicon Solutions  
a division of MIPS Technologies, Inc.  
1260 NW Waterhouse Ave., #100  
Beaverton, OR 97006-5794

503-597-5091 voice  
503-597-5099 fax  
Email: info@fs2.com  
Web: http://www.fs2.com/