

Preliminary Technical Data for SiliconBackplane Navigator™ On-Chip Bus Analyzer for Sonics SiliconBackplane μNetwork

The SiliconBackplane (SB) Navigator™ is used to monitor bus level intercommunication on Sonics SiliconBackplane μNetwork in System-on-Chip designs. It allows the user to capture real-time on chip SB activity along with related signals and display critical information for analysis on a PC. The system consists of an On-chip Instrumentation (OCI®) synthesizable logic block, a JTAG hardware probe, and PC based software for controlling probing and analysis. The OCI passively captures SiliconBackplane activity through the snoop port, monitors events, and buffers trace using on chip RAM. Collected trace information is transferred off chip through a JTAG port to the JTAG probe connected to a host PC. The host PC controls the collection process and displays captured bus history to the user with an easy-to-use graphical interface. The system runs on a Windows® 98/NT/2000/XP PC over an IEEE-1284 EPP/ECP high-speed parallel port. It provides a comprehensive debug tool for SiliconBackplane based systems at a competitive price.

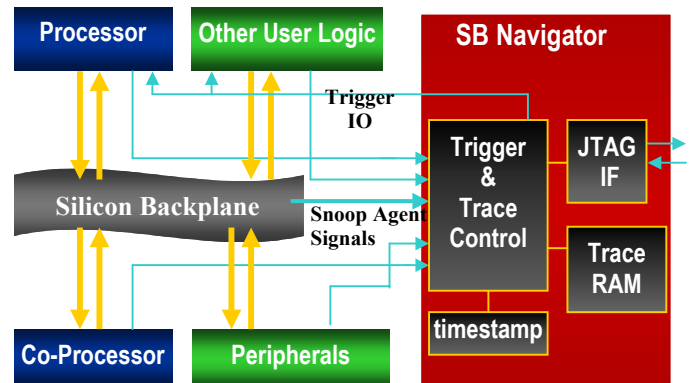
Bus Connection Overview

The OCI block is synthesized into the SoC design and can be used with either FPGA or Structured ASIC designs. It can support a range of SiliconBackplane configurations and multiple-master systems. The OCI block is pre-configured to monitor 179 SiliconBackplane signals, including 32 bit SB_addr and 64 bit SB_data, along with a range of standard supporting control signals. Additional SiliconBackplane sideband or user defined signals running over a common clock domain with SiliconBackplane can be concurrently traced, for additional on-chip visibility such as interrupt requests, processor, bus, or peripheral status, and control signals. The additional signals can also be used to recognize on-chip events and set system level triggers.

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Features Overview

- Captures bus activity in real-time
- Captures 179+ SB bus signals and additional user-defined inputs attached to other nodes in the SoC
- Bus clock mode trace stores SB signals on every clock
- Bus transfer mode filter aligns transfer cycles for single event triggering using combinations of address, data, and control
- Filtering of wait and idle state cycles in bus transfer mode
- Trace storage qualifiers; single cycle, start or stop trace on any trigger, counter, and state sequencer condition
- Configurable for user defined number of Processor cores
- Trace buffer stores bus cycles or bus transfers based on RAM memory size
- Up to 16 user defined triggers recognize combinations of 1, 0, X, signal values
- Sequential event monitoring using cascadable trigger states (2 to 16 states)
- Two 32-bit event counter/timers
- Trigger conditions include bus and user defined signals, Event counter/timer value and Trigger state
- Actions include Trigger, Trace control (start, stop, single), Trig Out control (pulse, assert, negate), Counter control (increment, start, stop, clear), and Goto state
- Trigger position variable in 1/512 increments of trace depth
- User definable timestamp records duration of each trace frame from trace start, displayable as absolute or delta times
- Automatic trace clock frequency measurement allows displaying frame durations in either nanoseconds or clocks
- Multiple external trigger in/out with configurable logic levels
- Easy-to-use graphical software interface with state views and waveform views of data
- Symbolic lookup and signal value naming for ease of bus signal viewing and analysis
- Optional VCD format export for simulation tools integration



Trace Features

SB trace is captured in an unfiltered **Bus Cycle Mode** where address, control, and data signals are captured on clock by clock basic. Trace depth is defined by available on chip RAM and can range from 4 to 32K frames deep.

The bus trace can be filtered real time into a **Bus Transfer Mode**, which aligns the trace based on transfer cycles. A Bus Transfer preprocessor align cycles of the SB operations to allow triggering on combinations of signals from the same transfer even though the signals occur in different clock cycles. Aligning relieves the user of the need to generate complex sequential triggers to recognize this type of event.

The alignment setting is also applied to the trace system. In this mode, bus fields valid at different times are recorded together, simplifying viewing of the bus activity. Operations can be dynamically switched between Bus Cycle and Bus Transfer mode on trace by trace basis

Trigger position can be set to user defined fraction of trace depth, to be able to look at both pre and post trigger events.

Triggering Features

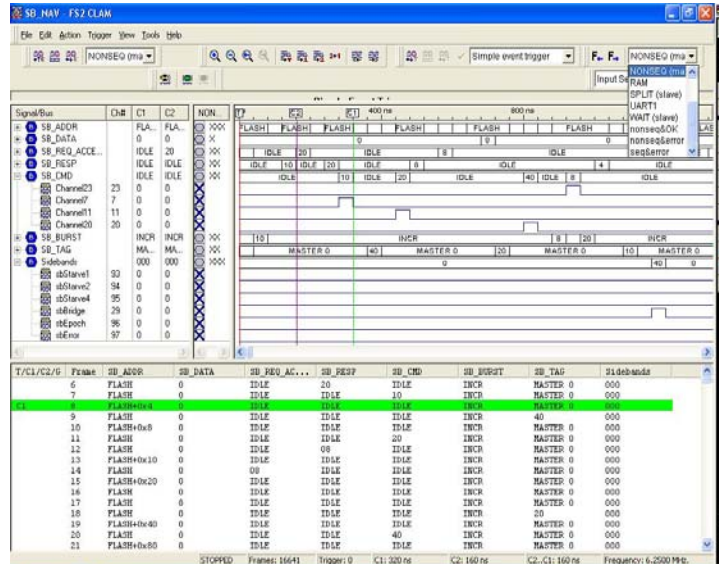
SB Navigator allows, during synthesis, selection of a configurable number (between 2 to 16) of triggers with configurable (between 2 - 16) numbers of states per trigger. Trigger conditions are AND combinations of three components, each are optional:

- Unfiltered or aligned bus comparator recognizing a high or low level or any edge on each signal,
- 32-bit counter matching a preprogrammed value,
- Trigger state

When a trigger condition is satisfied, one or more actions that affect the OCI or other parts of the SoC can be taken. These can include mark the trigger frame, turn trace on/off, record a single frame, turn the counter on/off, increment or clear counter, or assert the trigger interfaces or change trigger state. Trigger actions can in turn initiate some logic or control in the μ Network or at the core level. This wide variety of conditions and actions provides system flexibility and visibility into SiliconBackplane μ Network operations for monitoring and tuning System-on-Chip performance based on a range of parameters.

Host software

The host software runs on Windows based PCs. It displays trace in either a waveform or state table mode. All bus signals can be viewed either numerically or symbolically.



The user can define symbolic address ranges and display the symbol + offset when the address value matches the symbol.

The user interface also supports template based trigger window for set up of events, triggers, and trigger actions.

FS2 Command line interface

The SB Navigator also includes a command line interface (CLI). The CLI is based on the widely used Tcl/tk command language, which allows writing post-analysis programs, provides command recall, transcripts of previous activity, and batch script operations.

Host Requirements

Pentium class PC with minimum 32 Mbytes of memory, IEEE-1284 (EPP/ECP) parallel or USB port and Windows[®] 98/NT/2000/XP operating system are required.

Product Codes

NAV-SB/INT SiliconBackplane On Chip bus analyzer with internal trace capture



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