



Preliminary Technical Data for **OCP Navigator**TM On-Chip Bus Socket Analyzer for OCP Bus Systems

The OCP NavigatorTM is used to monitor signal activity at the OCP Socket level for in System-on-Chip designs. It allows the user to capture bus transfer activity along with related signals in real-time and display critical information for analysis on a host PC.

The system consists of an On-chip Instrumentation (OCI[®]) synthesizable logic block, a JTAG hardware probe, and PC based software for controlling probing and analysis. The OCI passively captures bus interface activity, buffers it using on chip RAM, and transfers the collected data off chip via a JTAG port to the JTAG probe. The host PC controls trace collection and provides captured bus history trace to the user with an easy-to-use graphical interface. The system runs on a Windows[®] 98/NT/2000/XP PC over an IEEE-1284 high-speed parallel port. It provides comprehensive debug tools for OCP compliant based systems at a competitive price.

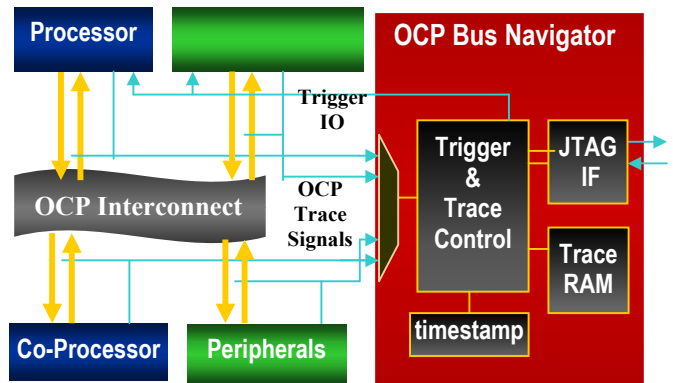
Bus Connection Overview

The OCI block is synthesized into the SoC design and can be used with either FPGA or Structured ASIC designs. It can support most OCP configurations and multiple-master systems. The OCI block monitors 144 signals (for 32 bit address/64 bit data OCP) including all critical control and status signals, plus command, burst, and tag extension signals. The OCP Navigator has a front-end multiplex logic, to allow either selection of an OCP Socket or selection of a set of control signals from all the sockets for triggering and trace. A user defined number of additional signals running over a common clock domain with the OCP bus, can be hooked up to nodes in the SoC such as interrupt requests, processor, bus, or peripheral status, and control signals. The additional signals can also be used to recognize on-chip events and set system level triggers.

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Features Overview

- Captures bus activity in real-time
- Captures 92-124 OCP bus signals and up to 120 additional user-defined inputs attached to other nodes in the SoC
- Bus clock mode trace stores OCP signals on every clock
- Bus transfer mode filter aligns transfer cycles for single event triggering using combinations of address, data, and control
- Filtering of wait and idle state cycles in bus transfer mode
- Trace storage qualifiers; single cycle, start or stop trace on any trigger, counter, and state sequencer condition
- Configurable for user defined number of OCP Masters
- Trace buffer stores bus cycles or bus transfers based on RAM memory size
- Up to 16 user defined triggers recognize combinations of 1, 0, X, signal values
- Sequential event monitoring using cascadable trigger states (2 to 16 states)
- Two 32-bit event counter/timers
- Trigger conditions include bus and user defined signals, Event counter/timer value and Trigger state
- Actions include Trigger, Trace control (start, stop, single), Trig Out control (pulse, assert, negate), Counter control (increment, start, stop, clear), and Goto state
- Trigger position variable in 1/512 increments of trace depth
- User definable timestamp records duration of each trace frame from trace start, displayable as absolute or delta times
- Automatic trace clock frequency measurement allows displaying frame durations in either nanoseconds or clocks
- Multiple external trigger in/out with configurable logic levels
- Easy-to-use graphical software interface with state views and waveform views of data
- Symbolic lookup and signal value naming for ease of bus signal viewing and analysis
- Optional VCD format export for simulation tools integration



Trace Features

OCP trace is captured in an unfiltered **Bus Cycle Mode** where all signals are captured on clock by clock basis. Trace depth is defined by available on chip RAM and can range from 4 to 32K frames deep.

Bus trace can be filtered real time into a **Bus Transfer Mode**, which aligns the trace based on transfer cycles. A Bus Transfer preprocessor aligns cycles of the OCP bus to allow triggering on combinations of signals from the same transfer even though the signals occur in different clock cycles.

Aligning relieves the user of the need to generate complex sequential triggers to recognize this type of event. Alignment also applied to the trace system. In aligned trace mode, bus fields valid at different times are recorded together, for a simpler view of the bus activity. Operations can be switched between Bus Cycle and Bus Transfer mode on trace by trace basis Trigger position can be set to user defined fraction of trace depth, to be able to look at both pre and post trigger events.

Triggering Features

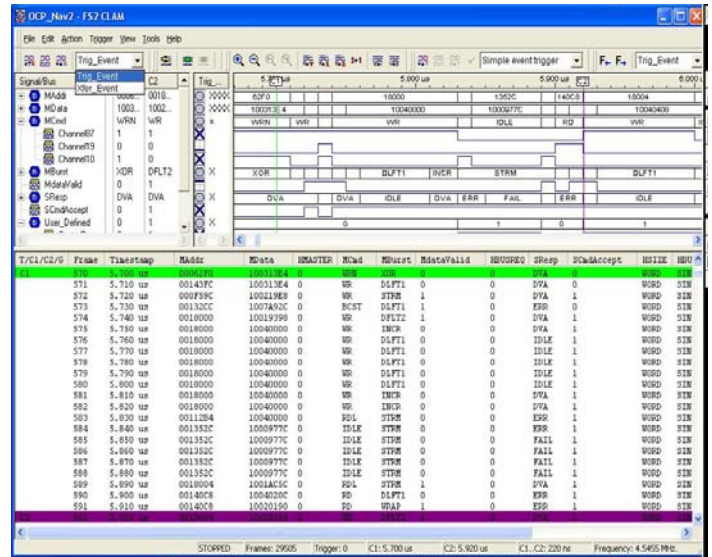
OCP Navigator allows, during synthesis, selection of a configurable number (between 2 to 16) of triggers with configurable (between 2 - 16) numbers of states per trigger. Trigger conditions are AND combinations of three components, each are optional:

- Unfiltered or aligned bus comparator recognizing a high or low level or any edge on each signal,
- 32-bit counter matching a preprogrammed value,
- Trigger state

When a trigger condition is satisfied, one or more actions that control the OCI or other parts of the SoC can be taken. These can include mark the trigger frame, turn trace on/off, record a single frame, turn the counter on/off, increment or clear counter, or assert the trigger interfaces or change trigger state. Trigger actions can in turn initiate some logic or control in the OCP network or at the core level. This wide variety of conditions and actions provides system flexibility and visibility into OCP operations for monitoring and tuning System-on-Chip performance based on a range of bus level parameters.

Host software

Windows based host software displays trace in waveform or state table formats. Bus signals can be viewed numerically or symbolically. The user interface supports template based windows for set up of events, triggers, and trigger actions.



Buses can define symbolic ranges and display a symbol + offset when a bus value matches the symbol. Predefined symbols for OCP control signals such as MCMMD, MRSP, MBURST, allow either numerical or symbolic display.

FS2 Command line interface

The OCP Navigator also includes a command line interface (CLI). The CLI is based on the Tcl/tk command language, which allows writing post-analysis programs, provides command recall, activity transcripts, and batch scripts.

Host Requirements

Pentium class PC with minimum 32 Mbytes of memory, IEEE-1284 (EPP/ECP) parallel or USB port and Windows® 98/NT/2000/XP operating system are required.

Product Codes

NAV-OCP/INT OCP On Chip bus analyzer with internal trace capture



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