



First Silicon Solutions

Technical Data for **ISA-JAZZ**

System Analyzer for Improv Systems Jazz DSP Cores

The System Analyzer is designed to support the special features and integrated peripherals of the Improv Systems Jazz DSP cores. Special “silicon hooks” for System-on-Chip development are integrated into the synthesizable IP model for the core. These On-Chip Instrumentation (OCI™) extensions allow FS2 to provide a powerful debug tool with advanced features at a competitive price.

The system analyzer is contained in a compact chassis that connects to the target system using a standard 20-pin debug connector. The system runs on a Windows® 98/2000/XP PC over an IEEE-1284 EPP/ECP high-speed parallel port.

Software Breakpoints

The system provides software breakpoints to be set in the Jazz processor writable address space.

Hardware Event Recognizers

Hardware execution breakpoints can be used to set breakpoints on types of instructions with masking to control which of the breakpoint fields should be included in the comparison. A databreakpoint is available for the data access address, value and cycle type. Hardware breakpoints can be used in writable space or in ROM or FLASH memory.

Features Overview

- Read-write all CPU registers, memory, and I/O
- Go, halt processor run control
- Supports multiple Jazz cores on the JTAG chain
- Single step by assembly instruction
- Supported by the Jazz debugger
- Software breakpoints supported
- Load binary, Intel Hex or S-record file formats
- One trigger-in/out signal to cross trigger with external instrumentation
- Low-level access to JTAG functions for silicon verification
- Flash programming support
- Single line assembler and disassembler
- Control Multiple Jazz DSP cores
- Hardware breakpoints for instructions and data



FS2 Command line interface

The ISA-JAZZ debugger includes a command line interface (CLI). The CLI can be used as both a user interface and also for writing sophisticated automated sequences of tasks for items like regression tests. The CLI is based on the widely used Tcl/tk command language.

Testing

For system verification, a loop-back board is provided which is plugged onto the target interface cable. A self-test exercises internal nodes and tests to insure the cable signal integrity.

Host Requirements

PC with minimum 32 Mbytes of memory, IEEE-1284 (EPP/ECP) parallel port and Windows® 2000/XP operating system are required.

Order Code: ISA-JAZZ



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