

Getting Started

FPGAView Altera

July 14, 2008



First Silicon Solutions
a division of MIPS Technologies, Inc.

document 10578.000
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1. Introduction

FPGAView, combined with the Altera FPGA tools, and a Tektronix logic analyzer (TLA) or Mixed Signal Oscilloscope (MSO), allows a designer to quickly and easily select one or more of several banks of internal FPGA signals for capture and analysis on a TLA or MSO. A single hardware debug port can be used to view up to 256 different banks of internal FPGA signals, which are routed to selected FPGA output pins via 'logic analyzer interface' multiplexers incorporated into the FPGA under test via the Altera Quartus II design application. FPGAView is used to select which banks of signals to route to the hardware debug port(s) and simultaneously update the TLA or MSO with the selected signals' logical names.

2. Setting Up the JTAG Interface

FPGAView requires a JTAG interface to the FPGA to be debugged. Prior to installing FPGAView, the Altera Qprogrammer or Quartus-II development environment must be installed on the same PC.

Altera provides several options for FPGA programming and control via JTAG. You have the option of installing the JTAG interface on a PC, or on the TLA itself. Once you have installed all the necessary Altera-provided drivers and software, connect the Altera JTAG interface to the board under test and to your development PC, or the TLA if you will be programming the FPGA from the TLA. If the JTAG interface is not connected to the machine running FPGAView, the JTAG server provided with the Altera tools must be enabled so remote access is possible.

A version of the Altera JTAG interface utilities that does not require a license is available at the following web address:

https://www.altera.com/support/software/download/programming/quartus2/dnl-quartus2_programmer.jsp?swcode=WWW-SWD-QPRG-51SP1-PC-SIN

3. Installing the Software

FS2 software is supplied on a CDROM or via the Internet. To install the software, insert the CDROM and run the setup.exe program found in the root directory on the CDROM. Software updates are supplied electronically via the FS2 website to licensed users. To install an update, download the appropriate EXE file, and then execute it.

FPGAView may be installed on a PC, or the TLA itself. For an MSO it must be installed on a PC. Installing on the TLA is often preferable if you do not have a workstation PC near the board to be tested. You will also need an Altera JTAG interface for controlling the FPGA from FPGAView, and for reprogramming the FPGA as you make changes to your design.

If FPGAView is installed on the TLA, the simplest configuration is to install the JTAG interface on the the TLA also. This requires only that the Quartus programmer software be installed on the TLA, not the entire Quartus II development environment.

If FPGAView is not installed on the TLA, and the JTAG interface is installed on the TLA, please refer to Appendix A. for details on configuring the TLA firewall to allow this configuration to work.

4. Setting Up the TLA or MSO

The TLA or MSO logic probes connect to the board under test via a debug port such as a Mictor38, connectorless board site, or a set of square pins. The debug port should be designed for easy connection to a logic analyzer. The signals available on the debug port are the outputs from the logic

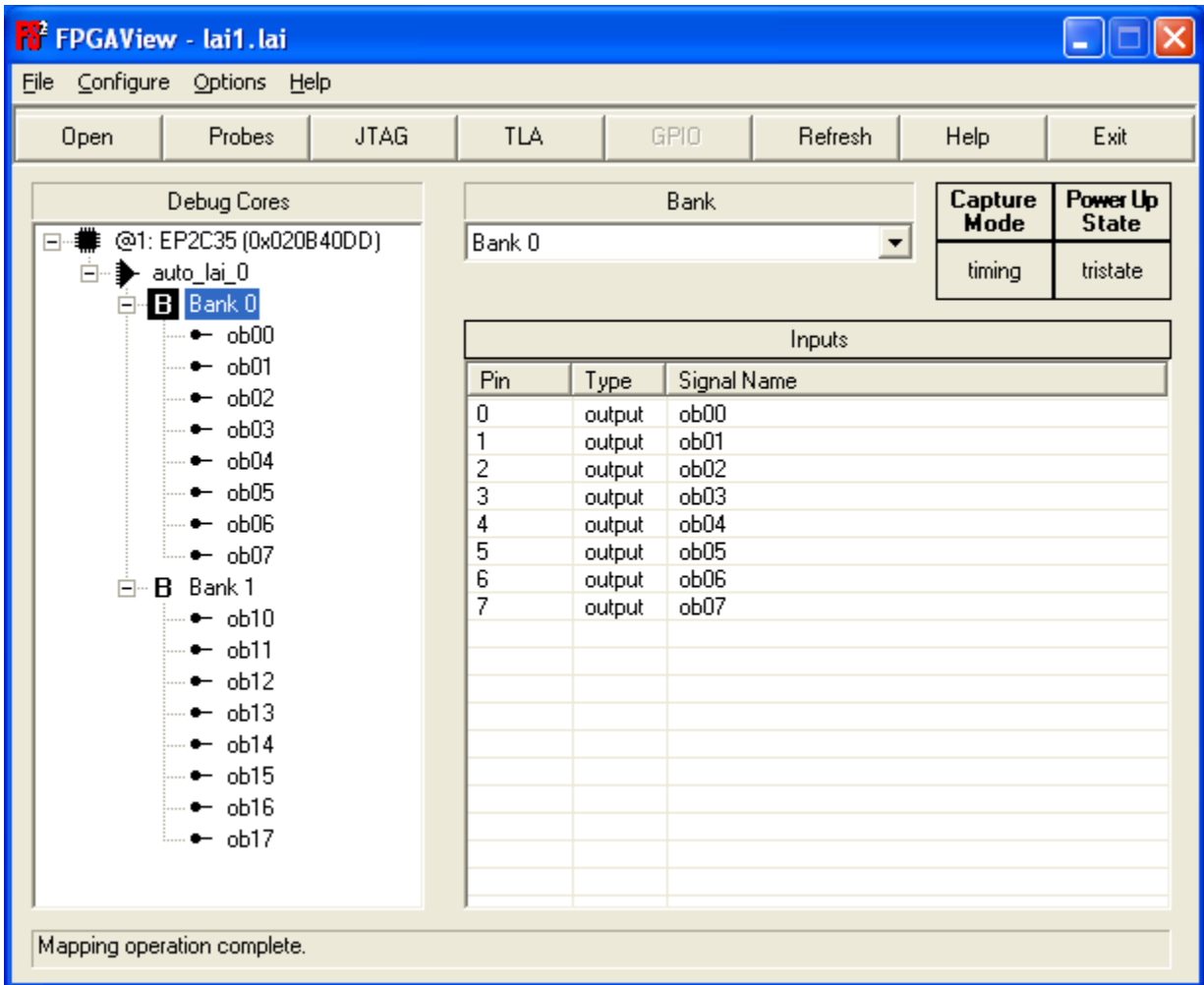
analyzer interfaces you create with the Altera Quartus II IDE. Once you decide which probe interfaces will be connected to the hardware debug port, you are ready to set up FPGAView.

For the case where FPGAView will be executed on a PC, it must be able to communicate with the TLA via a TCP/IP network connection.

For an MSO, the PC can connect up to it via network, USB port, or GPIB.

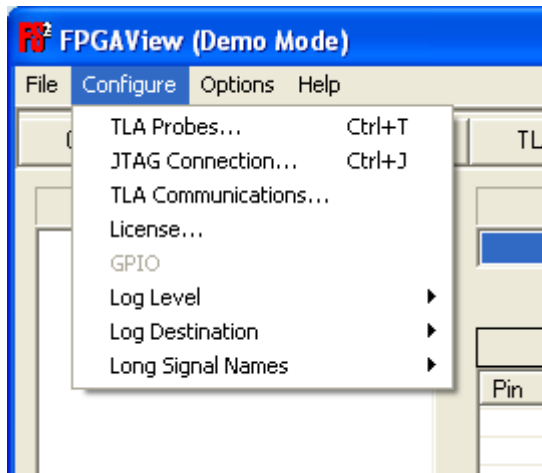
5. Setting up FPGAView

After starting FPGAView, you will see the main screen, which is both the main user interface for configuring the program, and for selecting which banks are to be routed to the TLA during development.

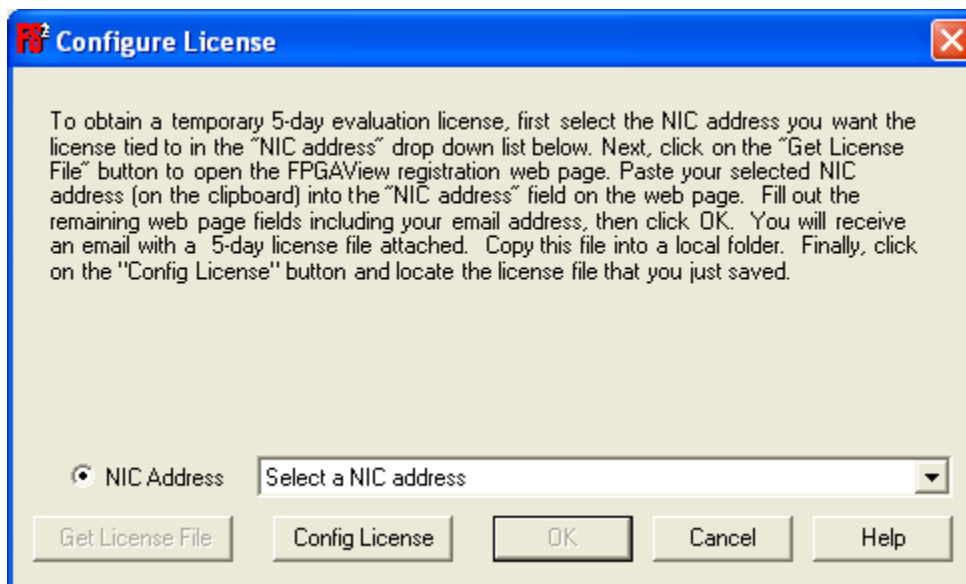


5.1. Licensing

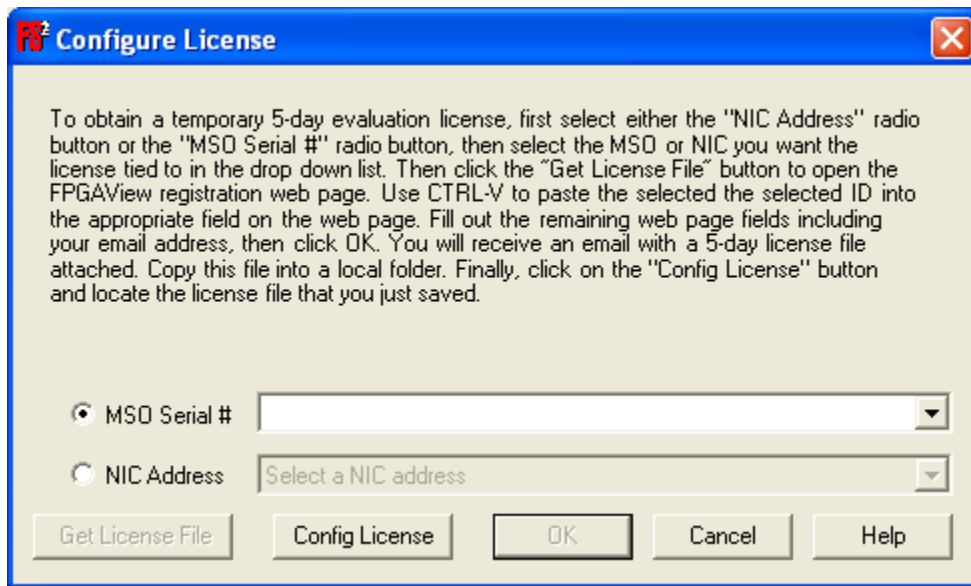
Prior to using FPGAView you must obtain a software license key. Select 'License...' from the 'Configure' menu entry.



If connecting to a TLA, the Configure License window displayed will be:



If connecting to a MSO, the Configure License window displayed will be:



The 'NIC address' field will contain one or more choices of NIC interfaces from which to choose. The NIC address is a 12 character value in the leftmost portion of the NIC address field.

The 'MSO Serial #' field will contain one or more choices of MSO instruments currently connected.

Click on the appropriate radio button to enable selection of the instrument you wish to associate with the license.

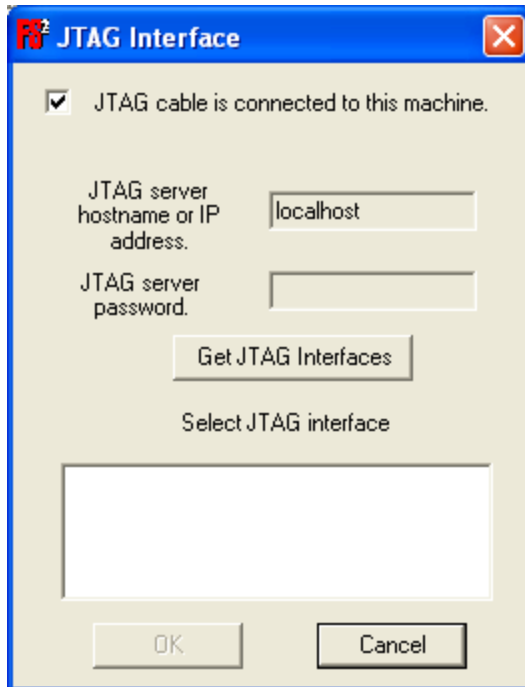
Clicking on the 'Get License File' button will open the FS2 FPGAView Evaluation Request webform. Put the cursor in the web form edit field labeled 'NIC Address' or 'MSO Serial #' and then select 'Paste' from the browser's Edit menu, or type Ctrl-v (hold the Ctrl key down and type the letter 'v'.) This will copy the NIC address or MSO serial number from the Configure License dialog into the web form. Repeat for the 'Confirm ...' field. Complete all required entries in the form, then click on the 'Request Evaluation License' button at the bottom of the form. A license key file will be emailed to you.

If you want to purchase a longer term license, contact FS2 sales. A license key file will be provided to you.

Copy the .lic license key file you receive to a directory of your choice on the machine on which FPGAView will be run. Click the 'Config License' button and use the file open dialog window to locate the license key file you just installed. Finally, click the 'OK' button to configure the license key. The software will be fully functional for the license period. After that, the software will only operate in 'Demo Mode', which will perform exactly the same as the licensed version, except you will not be able to switch signal banks in any FPGAs.

5.2. Target JTAG Connection

To configure the JTAG connection, click on the 'JTAG' button in the main window. The following window will be displayed:



If your JTAG interface hardware is located on the machine (PC or TLA) that is running FPGAView, make sure the 'JTAG cable is connected to this machine' check box is checked. Otherwise, enter the hostname or IP address of the machine that has the JTAG interface attached. You must also enter the password you set up when you configured the JTAG server on that machine.

Click 'Get JTAG Interfaces' to connect to the JTAG server. You should see the name of the JTAG interfaces appear in the listbox. If you don't see any JTAG interfaces listed, there is a problem with the network connection or the JTAG server. Refer to the Altera documentation for possible remedies.

Click on the JTAG interface device you wish to use and click 'OK' to close the window.

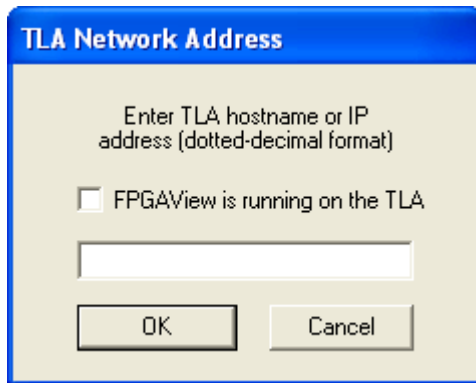
The devices connected to the JTAG chain will be automatically scanned and displayed in the 'Debug Cores' treeview list. Since this is the first time you are running FPGAView, you must identify the .LAI file which is associated with each device. The .LAI file is created with Quartus-II's Logic Analyzer Interface Editor.

Each device instance in the Debug Core list will be shown in red, indicating its associated LAI file is unknown. Click on each instance and a 'File Open' dialog box will be displayed to allow you to associate an LAI file. If the LAI files are located on another machine, you must have network access to that machine, and the LAI files must be located in a shared folder or subfolder that is accessible to the machine running FPGAView. Once the LAI file is located, FPGAView will remember the association so this operation will not have to be repeated. The device name and the logic analyzer interfaces contained in that device will now be displayed in black.

Click on any logic analyzer interface to show the signals and banks it controls.

5.3. TLA Connection


Click on the 'TLA Comm' button on the main window to configure the TLA connection. The following window will be displayed:



If FPGAView is running on the TLA itself, check the 'FPGAView is running on the TLA' checkbox. Otherwise, enter the IP address of the TLA in the edit window and click OK.

5.4. TLA Probe Configuration

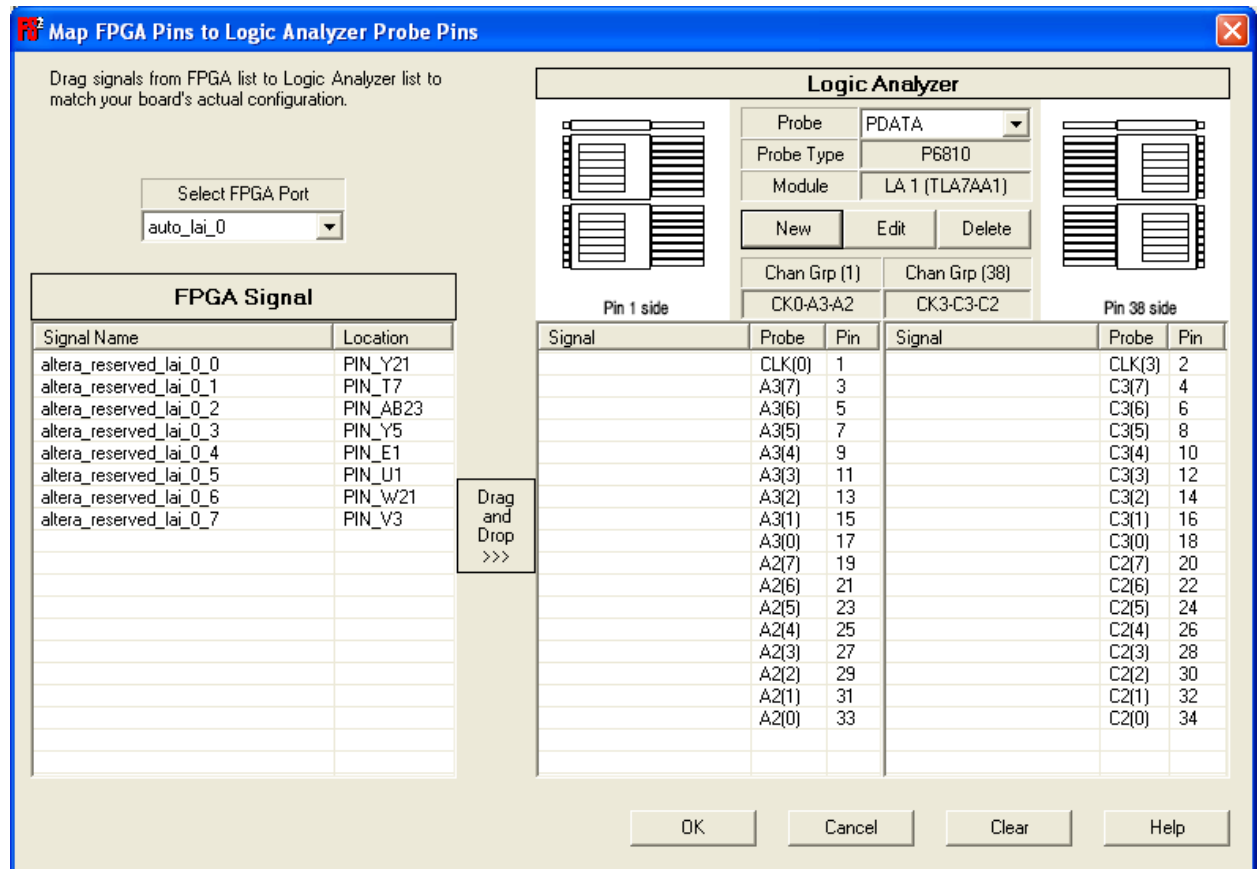
Once you have at least one LAI file identified, you can configure the TLA probes. First create the signal groups on the TLA that you will use to monitor the multiplexed signals connected to the logic analyzer interface outputs. When setting up the TLA signal groups, keep in mind that each logic analyzer interface can be configured for timing mode or state mode, but not both simultaneously. Group your signals accordingly.

First select one of the FPGA devices in the 'Debug Cores' treeview on the main window by clicking on one of its logic analyzer interfaces. These are marked with the  symbol.

Then, start the Probe Editor in FPGAView by clicking on the 'Probes' button on the main window. The following window will be displayed:

Enter a probe name of your choosing in the 'Probe Name' edit box. If you have multiple modules installed in the TLA, then select the module this probe is connected to from the 'Module' combobox. Then select the probe type from the 'Probe Type' list. Finally, choose the channel group that the probe is inserted into on the TLA from the list labeled 'Channel Group (pin 1)'. If the probe is a 34-signal probe with 2 distinct paddle connectors, also choose the second channel group from the 'Channel Group (pin 38)' list. If the probe is a single 34-pin paddle connector at the TLA end, the second channel group will be chosen automatically. Click OK to complete the probe definition.

After this operation you will see a Probe Mapping window resembling the following figure. Note that if you chose a 17-pin probe, the image and listbox on the right-hand side of the 'Logic Analyzer' section will not be displayed.



On the left side is a list called 'FPGA Signal', containing all the output signals connected to the logic analyzer interface selected in the list box labeled 'Select FPGA Port'. These are the signals you connect to the probe pins. These connections must match the physical layout of the board under test. You may wish to consult the schematics for your board for this operation.

The right-hand side contains the two probe signal definition listboxes. The first column in each will contain the names of the signals you connect from the FPGA Signal list. The second column contains the probe signal hardware names. These names are set when you defined the probe and selected which channel groups the probe cables occupy. The third column contains the probe pin numbers. You can reorder the signals in these lists by clicking on the column headings. Clicking on the 'Probe' column heading will reorder the list so the probe signal names are displayed in ascending order, which will make signal assignment easier, assuming your output signals are in ascending order.

To assign a signal, click on it in the 'FPGA Signal' list, hold down the left mouse button, and drag it over to the Probe signal lists, releasing the mouse button when the cursor is on the correct probe signal line.

To assign several signals at once, click on the first signal, hold down the Shift key and click on the last signal of the group you want to assign with the left mouse button. Hold the mouse button down and drag the signals to the right side list, and release the mouse button when the cursor is on the first line of the group of probe signals to which this group is to be connected.

You can continue to map signals from the currently selected device until you are done. To map more devices, click OK to save the current mapping and return to the main window. Then select another FPGA device before returning to the Probe Mapping window to continue mapping more signals.

If you make a mistake during the drag-n-drop operation, you can select the signals which were placed incorrectly (click-then-shift-click) and type the DEL key, or click on the 'Clear' button, to delete those signals from the probe definition. Clicking on the Clear button when no signals are selected will prompt you to delete all signal definitions from the currently selected probe. If you respond to the prompt by clicking on 'Yes'.

You can also drag-and-drop signals over existing signals, which replaces the previous signals with the new signals.

Click on the 'OK' button to save the signal mapping.

5.5. MSO Connection

The MSO is configured and controlled via TekVISA, Tektronix's instrument communications interface. The TekVISA software needs to be installed and configured prior to attempting to use FPGAView with the MSO. Please refer to the TekVISA documentation for detailed instructions. The key point is that TekVISA must be able to locate and identify your MSO before FPGAView will be able to communicate with it.

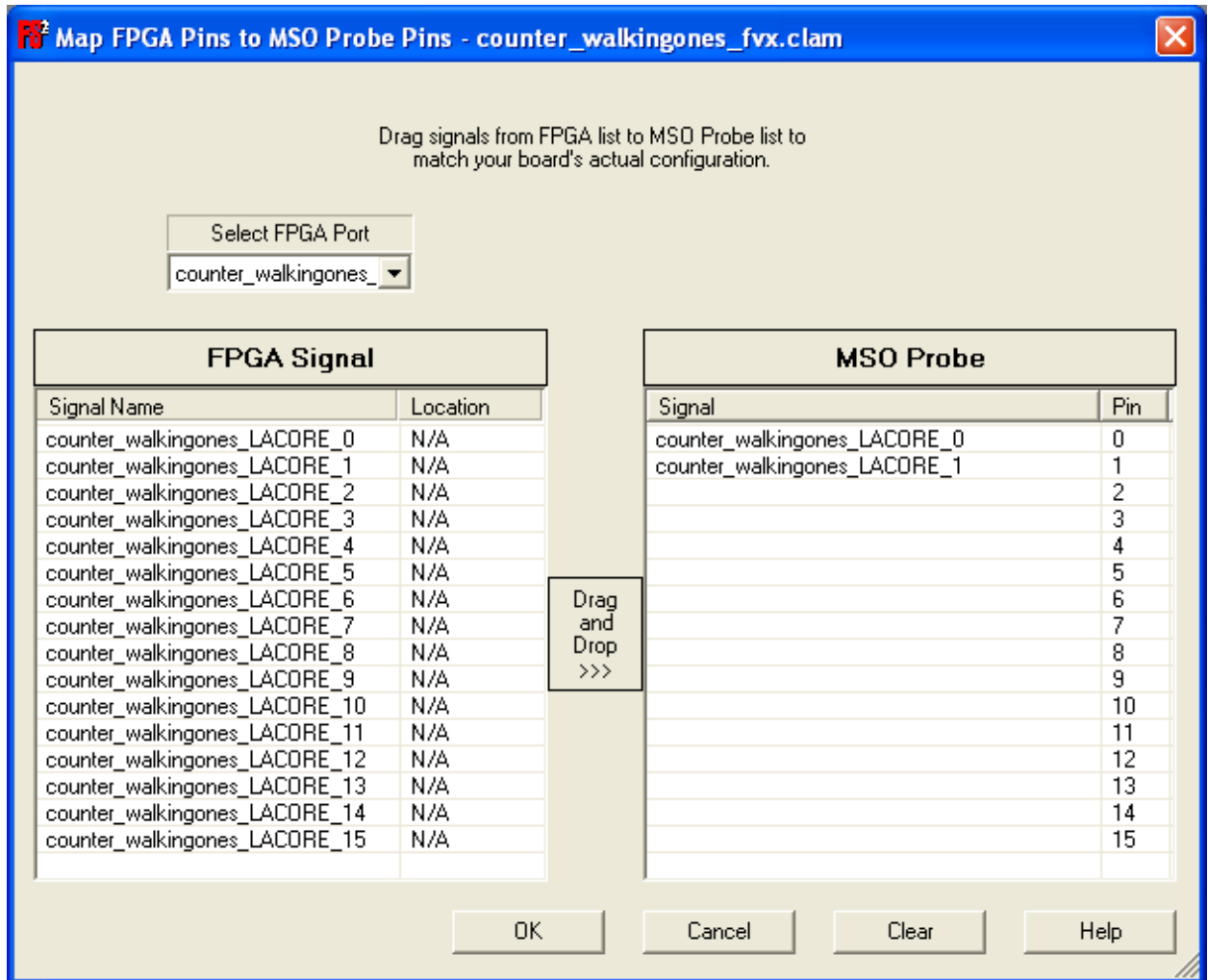
Once TekVISA is set up, start FPGAView with the FPGAView-Altera-MSO shortcut. FPGAView will automatically attempt to configure the available MSO's. You may also click the 'MSO' button. This will display the 'Connect to MSO' form.



Select the instrument to which you wish to connect, and click OK.

5.6. MSO Probe Configuration

Clicking on the 'Probes' button displays the 'Map FPGA Pins to MSO Probe Pins' form.



Map FPGA debug core output signals to MSO probe signals by selecting items from the FPGA Signal listbox and dragging them to the correct signals in the MSO Probe listbox, and click 'OK'.


The signals mapped to the MSO Probe can be removed by selecting them from the MSO Probe listbox and clicking the 'Clear' button, or by using the Delete key. Clicking 'Clear' when no signals are selected in the MSO Probe listbox will delete all the signal mappings from the MSO Probe listbox.



Click 'Cancel' if you do not want to keep the mappings. Click 'OK' to keep the mapping.


6. Using FPGAView

6.1. Switching Banks

Having survived the preceding setup procedures, it is time to use FPGAView for normal operation.

In the main window, in the 'Debug Cores' tree view all the FPGA devices which were found by the JTAG scan are displayed with the symbol . The first time a device is identified, it will be displayed in red, to indicate that no 'logic analyzer interface' (.lai) file has been associated with the device. Click on any device line to display an 'open file' dialog window and navigate to the folder containing your design files. Choose a .lai file to be associated with the device.

Once a .lai file is associated with a device, the banks () and signals () will be displayed automatically in the tree list each time the device is detected.

In the main window, click on any 'logic analyzer interface' line () to list all defined banks in the 'Bank' list, and that bank's signals listed in the 'Inputs' list.

Click on the arrow button at the right of the 'Bank' list to display all of the banks contained in the selected logic analyzer interface. Click on the bank to be connected to the TLA probe, and that bank will be selected, and the signal names will be sent to the TLA, which will display them next to the associated signals in any Waveform, Listing, or Setup window which contains the associated probe signal. You may also click on the bank line in the tree list to select the bank and send the signal names to the TLA.

6.2. Making Changes To Your Design

Any time a new design is programmed into the FPGA, you should click the 'Refresh' button in the main window. This will force the program to rescan the JTAG chain and detect all the devices and logic analyzer interfaces on the JTAG chain.

6.3. Making Changes to the TLA Signal Groups

Any time a change is made to the TLA signal grouping, FPGAView will automatically rescan the TLA for the new grouping configuration.

6.4. Associating a New LAI File

You may associate a new .lai file with a device by clicking on the device in the tree list. This will display an 'open file' dialog which you use to locate and select a new .lai file to associate with the device. If the FPGA device has not been programmed with the .lai file, you will be warned when you try to switch banks.

7. Saving and Restoring Settings

The menu selections under 'File' include 'Save' and 'Restore' selections. These menu items allow you to save probe definitions and debug core file associations you created during the current session, or restore these settings from a previously saved file. The settings are saved in files with the extension '.fvd' in the folder of your choice.

7.1. Saving Settings

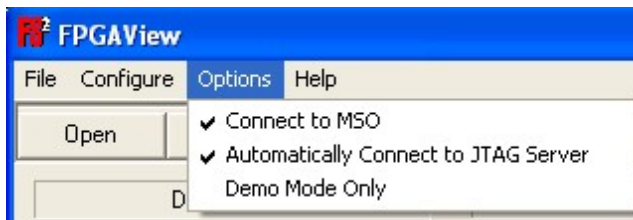
Save your current settings by selecting 'Save' from the 'File' menu. A dialog box will be opened to allow you to choose the folder and file in that folder in which to save the current session's settings. You may type a new name to save the settings in a new file (file extension is not required.)

7.2. Restoring Settings

You may restore previous settings by selecting 'Restore' from the 'File' menu. A dialog box will be opened to allow you to choose the folder and file in that folder from which the saved settings will be obtained.

8. Options

Under the menu item 'Options' are the following items:



8.1. Connect to TLA or MSO

This option, when checked, will cause FPGAView to attempt to connect to the TLA or MSO at startup, once the TLA or MSO connection information has been configured. Pressing the ESC key during the connection attempt will cancel the connection attempt. You may click the 'TLA' or 'MSO' button on the main form, or click the menu item Configure > TLA Communications... or Configure > MSO Communications... to configure the TLA network address or select the MSO instrument and attempt to reconnect.

8.2. Automatically Connect to JTAG Server

This option, when checked, will cause FPGAView to attempt to connect to the JTAG server at startup, once the JTAG server information has been configured.

8.3. Demo Mode Only

This option, when checked, will operate FPGAView in demo mode. In demo mode, no attempt will be made to connect to the JTAG server, and therefore no bank switching will occur. The signal names will be sent to the TLA or MSO though, so this mode is useful for demonstrating the program when there is no test hardware available or the JTAG server is not set up or available.

Deselecting Demo Mode, by unchecking the Demo Mode menu item, will revert the program back to normal mode, and will cause the JTAG connection to be reestablished immediately. If a valid license is not found, the program will require that a valid license key be obtained and entered before Demo mode is turned off.

If a JTAG connection cannot be established, the program will revert to Demo mode once again, and it will be necessary to turn Demo mode off manually before the program will try to reestablish the JTAG connection.

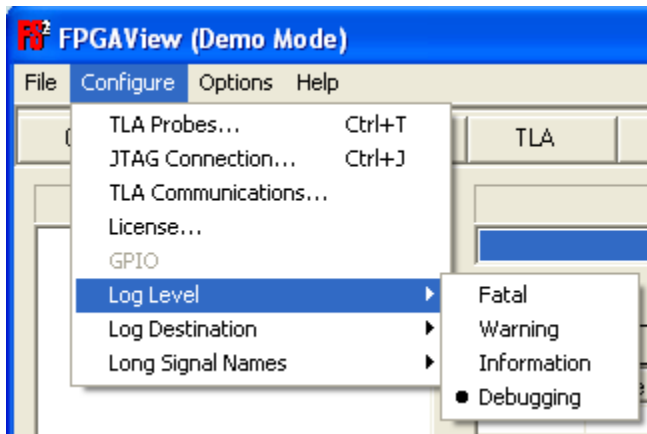
9. Error Logging

FPGAView logs significant events to the Application Event Log. To control the amount and type of messages logged, use the menu 'Configure...Log Level'. The four logging levels are:

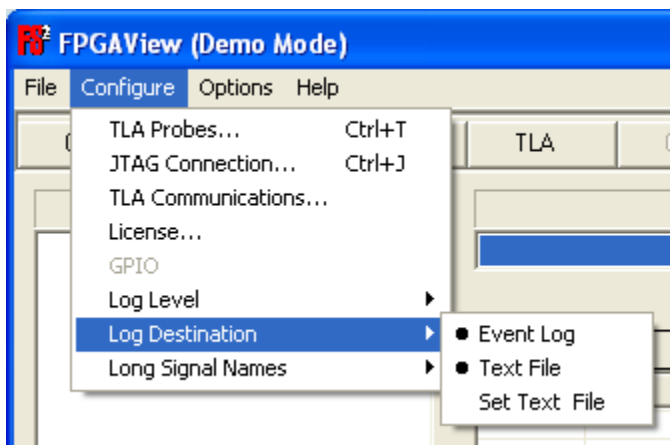
- Fatal – Only those errors that prevent FPGAView from continuing to operate are logged.
- Warning – Both fatal errors and those errors that may indicate a problem with FPGAView are logged.
- Information – Fatal, Warning and informative messages are logged.

- Debugging – Fatal, Warning, Informative and messages intended for detailed debugging are logged. Use this selection to obtain information for use by FS2/MIPS technical support personnel.

Normally, you should set the logging level to Fatal or Warning, to prevent the event log from filling too quickly.



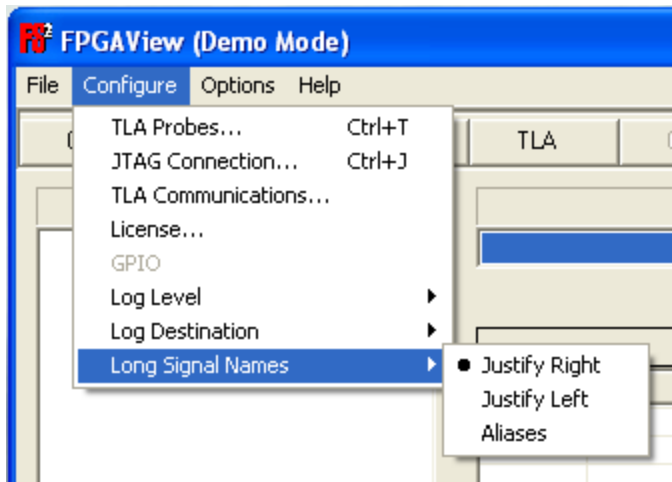
Use the 'Log Destination' to enable logging to the Application Event Log (use Administrative Tools Event Viewer to view these,) or to a text file, or both. Use the 'Set Text File' menu item to change the file to which the log messages are written.



10. Long Signal Names

The Configure menu contains a submenu to configure the display of long signal names. Some signal names generated by the ISE may be too long to display in a meaningful way on certain instruments. For instance, the MSO can only display 32 characters for a signal name. In such situations, it is sometimes better to display the trailing part of a signal name. The 'Long Signal Names' configuration menu allows you to choose:

- Left-justified signal name display (default) with the first character in the name always visible.
- Right-justified signal name display, with the last character in the name always visible.
- Aliases, where any aliases entered in the Quartus-II Logic Analyzer Interface configuration form are used in preference to the long signal names generated by Quartus.



11. Help

The Help button and the Help menu item 'FPGAView Help' display this document.

The Help menu item 'About' displays the software version, and a web link to FS2.com.

Appendix A. Using the TLA as the JTAG Server

If you are running the JTAG server and FPGAView on the same machine (TLA or PC), skip this section as it does not apply to your configuration.

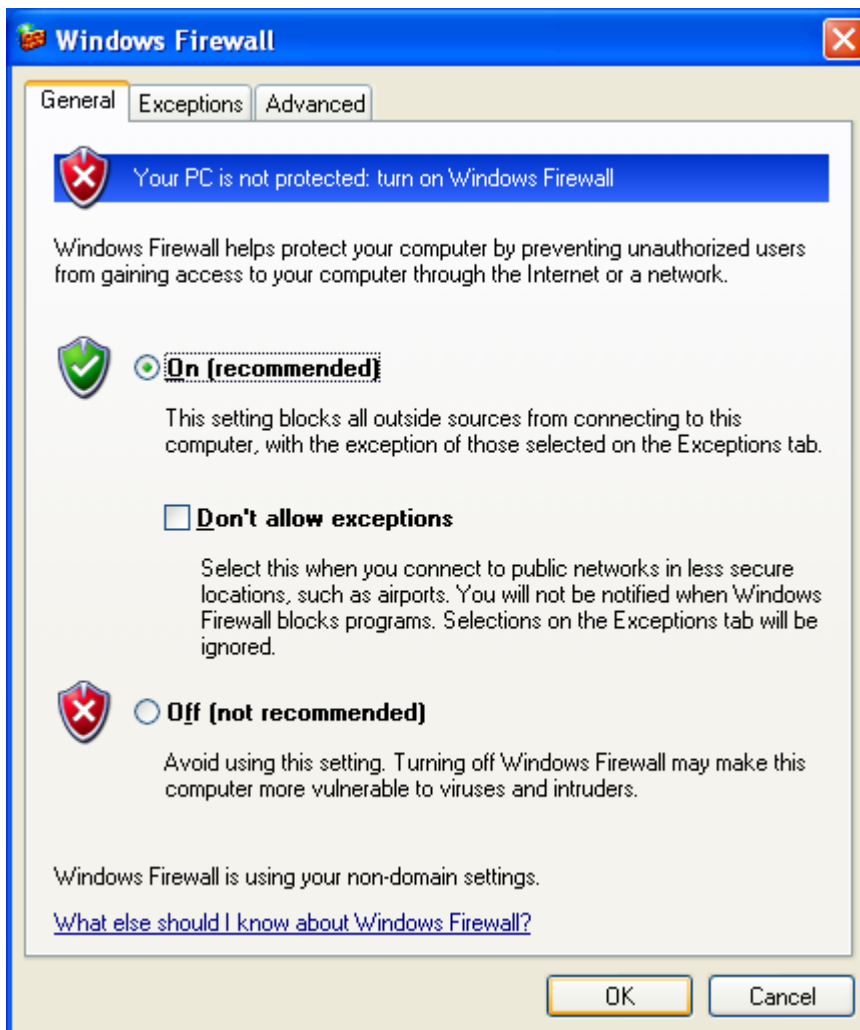
The TLA may be used as the JTAG server if it is properly prepared. First, the JTAG server must be enabled and configured to accept remote connections. Please refer to the Altera documentation for instructions on how to do this.

If the TLA operating system is Windows XP, the Windows firewall will probably be active. The firewall will prevent the JTAG server from accepting connections from remote machines, such as the PC which is running FPGAView.

To allow communications with the server on the TLA, it may be necessary to reconfigure the Windows firewall on the TLA machine. You must be logged in as an administrator to perform this operation.

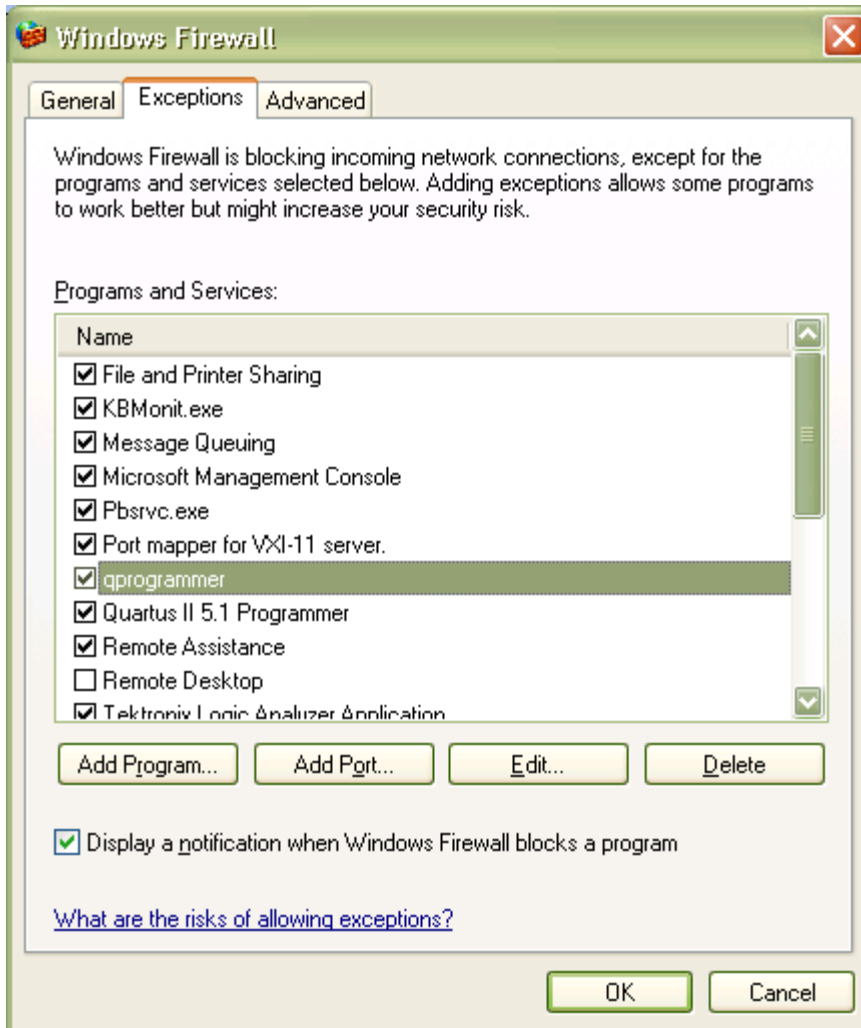
Start the Windows Security Center by clicking 'Start', then 'Control Panel', and double-click 'Windows Firewall'.

The following window will be shown:

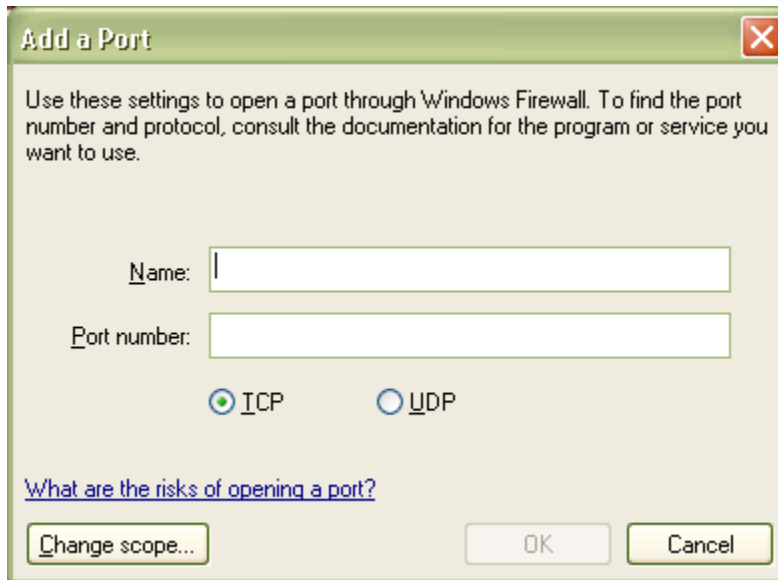


If the 'On (recommended)' radio button is not marked (empty), then you do not need to continue, so click on the Cancel button in this window and also in the Security Center window. You are done.

If the 'On' radio button is marked, uncheck the 'Don't allow exceptions' checkbox, if necessary, and then click on the 'Exceptions' tab. The following window will be shown:



Select 'qprogrammer', making sure it is checked, and click on 'Add Port', which will display the following window:



Enter 'qprogrammer' in the Name edit box, and 1309 in the Port number edit box, and select TCP, then click OK, then click OK in the previous window, and close the Security Center application window. Now the Quartus JTAG programmer on the TLA should be accessible from FPGAView running on another machine in the network.