

FS2 Logic Navigator[®]

FAQ

For Actel Devices

January 19, 2005



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1. What is the Logic Navigator?

The FS2 LOGIC NAVIGATOR[®] is a Configurable Logic Analyzer System consisting of on-chip instrumentation (RTL) IP, external hardware and software. The on chip IP routes internal signals in the designer's HDL code to internal or external trace memory where the signals are buffered and then to a Windows based GUI where they can be examined. Trigger events and other configuration parameters can be set up by the designer to control which signals are recorded in memory and the conditions for capture. Trigger and trace memory may be implemented either inside the FPGA (on chip or Internal Logic Navigator) or externally in a dedicated trace and debug probe (off chip or External Logic Navigator).

Note that in most FS2 Logic Navigator documents, On-Chip and Internal are referred to interchangeably and Off-Chip or External are referred to interchangeably with regards to instrumentation IP and probes.

2. Is there more than one version of the FS2 Logic Navigator?

Yes, there are two versions – On-Chip or Internal Logic Navigator and Off-Chip or External Logic Navigator.

The On Chip Logic Navigator is designed to provide logic debug for Actel ProASIC and ProASIC^{PLUS} FPGAs via the JTAG port using the FlashPro family of programmers as logic analyzer probes. Other devices are supported via a separate JTAG TAP (all IP for this is included in the Logic Navigator release) and FS2 JTAG probe.

Off-Chip Logic Navigator streams trace information externally via a parallel trace port interface to a dedicated FS2 Logic Navigator probe for trace post processing and buffering.

The Internal JTAG Logic Navigator Probe does not support External Logic Navigator IP and External Logic Navigator Probe does not support Internal Logic Navigator IP.

3. What are differences between the External and Internal Logic Navigator?

The External Logic Navigator instrumentation IP contains no event recognition logic and uses no on-chip memory to trace data, which reduces logic and area requirements on the user's design. Instead, all data is routed off-chip to an FS2 Logic Navigator Probe. The Logic Navigator Probe has complex event recognition logic enabling the designer to create complex trigger events. The Probe also has an extensive trace memory allowing the designer to store more trace cycles than Internal Logic Navigator, without using any additional on-chip resources. The External Logic Navigator IP requires from 2 to 35 external device pins, depending on the configuration and the number of signals being traced.

The Internal Logic Navigator instrumentation IP uses event recognition logic and trace memory in the designer's chip to hold trace data and control logic to start, stop and read the trace memory. The internal Logic Navigator supports a wide range of user customization of features and parameters. Internal Logic Navigator communicates through a JTAG port, in the case of APA devices, the same JTAG port used for programming, independent of how many signals are being traced. A FlashPro or FlashPro Lite Programmer is used to configure the Logic Navigator control logic on the chip and to route data from the on-chip trace to a Windows PC.

4. What are 1x, 2x and 4x configurations of the External Logic Navigator?

The External Logic Navigator IP comes in 3 different configurations: 1x, 2x and 4x. The 2x and 4x configurations of the Logic Navigator can be used to reduce the number of package I/O pins required by the Logic Navigator but requires the use of an on-chip PLL.

In the 1x configuration, a single, system wide clock is used for all data and control registers. The number of device I/O pins required by the 1x IP configuration will be equal to the number of data signals being traced plus control signals.

In the 2x configuration, the Ext. Logic Navigator IP uses two clocks; a system clock used by control and data registers (same as 1x configuration) within the Logic Navigator and a second clock (twice the frequency of the system clock) used to clock the data I/O registers. The number of data I/O pins required by the 2x configuration is half that of the 1x configuration. The 2x configuration reduces the number of I/O pins by multiplexing the trace data to the I/O pins such that data is being clocked at twice the frequency of the system clock, but at half the width.

In the 4x configuration, the Logic Navigator IP again uses two clocks; a system clock used by control and data registers (same as 1x configuration) within the Logic Navigator and a second clock (4x the frequency of the system clock) used to clock the data I/O registers. The number of data I/O pins required by the 4x configuration is one fourth that of the 1x configuration. The 4x configuration reduces the number of I/O pins by multiplexing the trace data to the I/O pins such that data is being clocked at 4 times the frequency of the system clock, but at one fourth the width.

Both 2x and 4x configurations require synchronization between both clocks, which typically is done using an on chip PLL. They are not appropriate for designs that do not have clock doubling resources such as PLLs.

5. Is the Logic Navigator IP available in both Verilog and VHDL?

Yes. Both Verilog and VHDL design flows are fully supported. Verilog and VHDL source files are provided for both the Internal and External Logic Navigator instrumentation IP. A supporting OCI Generator tool is provided as part of the Logic Navigator release that supports configuration, instantiation, and integration of Logic Navigator IP for either Verilog or VHDL design flows.

6. How do I set up my design to use External or Internal Logic Navigator IP?

The Logic Navigator probe hardware and cable connectors are different between the internal and external Logic Navigator systems. A designer needs to first determine which system is appropriate for the design. This decision is based on tradeoffs of available FPGA gates vs. chip IO, debug features required, and overall cost of debug.

The designer then instantiates the external or internal module in the design as required, preferably using the OCI Generator tool. Details for instantiation are discussed in External Logic Navigator ISS (Instantiation, Simulation, and Synthesis) and Internal Logic Navigator ISS documents respectively.

7. How do I simulate or synthesize Logic Navigator IP in my design?

A design that includes Logic Navigator instrumentation IP should be treated as independent from the original design. The synthesizable source files for all instrumented blocks should be included in the design.

The instrumented design files will have a Inavint or Inavext suffix in both the file name and entity or module name of the instrumented files. The Logic Navigator RTL IP should also be instantiated during simulation or synthesis. The internal Logic Navigator RTL IP files typically have a clam2 prefix on the file name and entity or module. The external Logic Navigator RTL IP are all in files Inav_ext.v and Inav_ext.vhd and have entity or module names of clamext1x, clamext2x, clamext4x.

More information is provided in the Internal Logic Navigator ISS and External Logic Navigator ISS documents respectively.

8. How many signals can the FS2 Logic Navigator simultaneously monitor?

The Internal Logic Navigator can simultaneously monitor one input set consisting of up to 256 signals.

External Logic Navigator can simultaneously monitor one input set consisting of up to 32 signals.

Internal Logic Navigator allows up to 16 input sets to be routed into the Logic Navigator. This gives a total of up to 4096 signals which can be selectively monitored.

External Logic Navigator allows up to 4 input sets to be routed into the Logic Navigator. This gives a total of up to 128 signals which can be selectively monitored.

The user can configure the Logic Navigator via the FS2 software at run time to select which of the input sets is to be monitored.

9. What size trace memory does the Logic Navigator IP support?

The External Logic Navigator supports a memory depth of 128K words.

The Internal Logic Navigator IP supports a memory depth from 16 to 64K words (this is highly dependent on the amount of on chip RAM available in a device that can be configured as trace memory).

10. How many trigger events are supported?

The External Logic Navigator supports 4 trigger events.

The Internal Logic Navigator IP is configurable for 2, 4, 8, or 16 trigger events determined when the designer instantiates the Verilog or VHDL code into the design.

11. Which Actel devices are supported?

External Logic Navigator contains no code that is specific to any Actel device line and supports all devices.

Internal Logic Navigator has 2 modes of configuration that are based on RTL files selected:

1. a JTAG interface that is specific to ProASIC^{PLUS} device line, and
2. a general purpose JTAG TAP interface. The Logic Navigator JTAG TAP IP contains no code that is specific to any device line and JTAG TAP configuration of Logic Navigator IP will support Actel technologies (including antifuse), provided that the devices support gate and memory requirements for Internal Logic Navigator.

12. Which EDA tools are supported?

The FS2 Logic Navigator IP has been verified by FS2 to flow without error through the Actel Libero software. This includes Modeltech ModelSim for simulation and Synplicity Synplify Light for synthesis. Logic Navigator IP has also been verified on Mentor Leonardo for synthesis.

13. What range of clock frequencies does the Logic Navigator support?

Below is a table showing the minimum and maximum frequencies for different versions of the Logic Navigator IP.

Table 3. LOGIC NAVIGATOR IP Timing Specifications

| LOGIC NAVIGATOR Version | Max Trace Width | Min System Frequency | Max System Frequency | Max Output Width | Max TrcClk Frequency |
|-------------------------|-----------------|----------------------|-----------------------|------------------|----------------------|
| 1X | 32 | 50 MHz | 100 MHz | 32 | 50 MHz |
| 1X-slow | 32 | 0.0 MHz | 50 MHz | 32 | 25 MHz |
| 2X | 32 | 25 MHz | 100 MHz | 16 | 100 MHz |
| 2X-slow | 32 | 0.0 MHz | 25 MHz | 16 | 25 MHz |
| 4X | 32 | 12.5 MHz | 66 MHz | 8 | 132 MHz |
| 4X-slow | 32 | 0.0 MHz | 12.5 MHz | 8 | 25 MHz |
| Internal | 32 | 0.0 MHz | Depends on technology | NA | NA |

14. How many logic tiles does the Logic Navigator IP use?

External Logic Navigator varies between 36 and 132 Actel Logic tiles depending on the off chip instrumentation configuration selected. A table of area vs. off-chip Logic Navigator configurations is given in Appendix B of the External Logic Navigator ISS document.

Due to the wide range and number of configuration parameters in internal Logic Navigator, the number of logic tiles can vary significantly. A minimal on chip Logic Navigator IP configuration is on the order of 850 logic tiles for 8 bit wide trace, 1100 logic tiles for 16 bit wide trace, and 1500 logic tiles for 32 bit wide trace.

A table of area vs. on-chip Logic Navigator configurations is given in Appendix B of the Internal Logic Navigator ISS document.

15. Do I need to add synthesis timing constraints for Logic Navigator IP?

In order for the FS2 Logic Navigator IP to meet the timing specifications, it may be necessary to add timing constraints to the design. The Logic Navigator ISS documents contain detailed explanations and examples of the constraints that should be included.

16. Is there a demo design available?

Yes. The code for a fully operational top-level design is included in the file sets for both Verilog and VHDL. A designer is free to use this design as a starting point or a reference if desired.

17. How do I customize the Logic Navigator IP?

The Logic Navigator code is parameterized such that the designer can fully customize the Logic Navigator IP by driving the desired parameter values from his or her code without the need to alter a single line of code within the FS2 Logic Navigator. FS2 does not recommend that a designer make changes to the Logic Navigator IP.

18. Where can I get more detailed information on using Logic Navigator IP?

The FS2 Logic Navigator product release contains a Getting Started document, an ISS (Instantiation, Simulation and Synthesis) Guide and an OCI Generator User Guide. The ISS document contains detailed descriptions, along with examples, of how to use the Logic Navigator IP in your design.

Specific questions on Logic Navigator and its use may be directed to support@fs2.com.